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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/742,036 | 12/20/2000 | Toshiyuki Matsuzaki | TIJ-29142 | 8675 |

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| EXAMINER |
|---|
| SHAPIRO, LEONID |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2673 | |

DATE MAILED: 03/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/742,036 | Applicant(s) MATSUZAKI, TOSHIYUKI |
|---|---|---|
| | Examiner Leonid Shapiro | Art Unit 2673 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

## *Specification*

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure also is objected to because it has two portions "Problem" and "Solution Means". Words "Problem" and "Solution Means" need to be removed. Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities: On Page 9, Line 11 data bus 220 mentioned, should be data bus 200, as in Fig. 4A. On the page, Line 13, a cross-sectional view along line A-A' mentioned. In Fig. 4A it is "4B". On Page 10, Lines 19, 22 pad units should be 130a instead of 132.

Appropriate correction is required.

## *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5, 8-9 rejected under 35 U.S.C. 103(a) as being unpatentable over Dingwall (US Patent No. 5,739,805) in view of Mical et al. (US Patent No. 6,191,772 B1).

As to claim1, Dingwall teaches a module for a display device that has a semiconductor chip that has n (wherein n is a natural number and n>=2) signal input terminals as well as n input terminals to be connected respectively to n signal input terminal (See Fig. 4, items 210, DATA (9:0), in description See Col. 5, Lines 23-28), a drive signal generation circuit that generates drive signals that drive a display device based on image signals output from the output terminals and m (wherein m is a natural number and m>=2) signal output terminals for outputting drive signals substrate that includes n terminals and n first lines that connect input terminals and signal input terminals of semiconductor chip respectively, and m output terminals and m second lines that connect output terminals and the signal output terminals of semiconductor chip respectively, and on which semiconductor chip mounted (See Fig. 9, items COL #1-#128, in description See Col.10, Lines 54-62); first and second substrate that includes n-sets of signal terminals that correspondent to the n terminals of first substrate and n sets of lines that sequentially connect the first trough n-th signal terminals, and by which n signal terminals are connected are connected to the n terminals of the first substrate (See Fig. 4, items 210, DATA (9:0), in description See Col. 5, lines 23-28).

Dingwall do not teach switching circuit that sequentially connects first through n-th input terminals to first through n-th output terminals respectively when a control signal is at the

first logical level and sequentially connects first through n-th input terminals to first through n-th output terminals respectively when a control signal is at the second logical level.

Mical et al. teaches cross-over unit which can place appropriate even or odd-numbered pixel signals on respective side buses (See Fig. 1, items 150, 151, 154 , in description See Col. 13, Lines 46-63). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Mical et al. approach in the Dingwall apparatus applying it to first through n-th input terminals to first through n-th output terminals respectively in order to avoid the need of a row buffer (See Col. 3, Lines 51-54 in Mical et al. reference).

As to claim 2, Mical et al. teaches cross-over unit which can place appropriate even or odd-numbered pixel signals on respective side buses (See Fig. 1, items 150, 151, 154 , in description See Col. 13, Lines 46-63). It would have been obvious to one of ordinary skill in the art at the time of invention to implement Mical et al. approach in Dingwall apparatus applying it to the logical level of the control signals supplied to semiconductor chip arranged corresponding to odd and even numbers are in reverse of each other in order to avoid the need of a row buffer (See Col. 3, Lines 51-54 in Mical et al. reference).

As to claim 3, Dingwall teaches n-sets of signal terminals of second substrate are arranged linearly approximately in a row, and m output terminals are connected to signal electrodes of LCD (See Fig. 4, items 210, DATA (9:0), in description See Col. 5, Lines 23-28, Fig. 9, items COL #1-#128, in description See Col.10, Lines 54-62);

As to claims 5, 8-9, Dingwall teaches input terminals of first substrate and the signal terminals of second substrate include a first terminal and second terminal respectively, the first line of first substrate includes a first wiring part that connects first terminal and the signal input

terminal of semiconductor chip and a second wiring part that connects second terminal and signal input terminal of semiconductor chip, and the wiring of the second substrate connects second terminal and first terminal in signal terminals of adjacent sets (See fig. 4, items 210, DATA (9:0), in description See Col. 5, lines 23-28).

5. Claims 4, 6-7, 10, rejected under 35 U.S.C. 103(a) as being unpatentable over Dingwall and Mical et al. as aforementioned in claims 1-3 in view of Voisin et al. (US Patent No. 5, 680, 191).

As to claims 4, 6-7, Dingwall and Mical et al. do not show the first substrate is a flexible substrate.

Voisin et al. teaches the first substrate is a flexible substrate (See Figs. 3-4, item 50, in description See Col. 11, Lines 12-15). It would have been obvious to one of ordinary skill in the art at the time of invention to implement approach as shown by Voisin et al. in Dingwall and Mical et al. apparatus.

As to claim 10, Dingwall teaches input terminals of first substrate and the signal terminals of second substrate include a first terminal and second terminal respectively, the first line of first substrate includes a first wiring part that connects first terminal and the signal input terminal of semiconductor chip and a second wiring part that connects second terminal and signal input terminal of semiconductor chip, and the wiring of the second substrate connects second terminal and first terminal in signal terminals of adjacent sets (See fig. 4, items 210, DATA (9:0), in description See Col. 5, lines 23-28).

*Conclusion*

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

The Jeong (US Patent No. 6,335,721 B1) reference discloses LCD source driver.

The Matsuda et al. (US Patent No. 5, 886, 679) reference discloses driver circuit for driving LCD.

The Okada et al. (US Patent No. 5, 686, 933) reference discloses drive circuit for a display apparatus.

*Telephone inquiry contact*

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

ls
February 21, 2003

BIPIN SHALWALA
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2600